REMARKS

This Amendment responds to the Office Action dated October 19, 2005 in which the Examiner rejected claims 25-36 under 35 U.S.C. §112 first and second paragraphs and rejected claims 25-33 under 35 U.S.C. §103.

As indicated above, claims 25 and 31 have been amended to contain subject matter described in the specification. Applicants respectfully submit that no new matter has been added. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 25-36 under 35 U.S.C. §112 first paragraph.

As indicated above, claims 25-36 have been amended in order to more particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. Therefore, Applicants respectfully request the Examiner withdraws the rejection to the claims under 35 U.S.C. §112, second paragraph.

Claim 25 claims a semiconductor device claim 31 claims a method of manufacturing a semiconductor device. The semiconductor device comprises an active area, an insulating film defining the active area and a current/leakage prevention portion. The active area has a recess defined by first, second, third, fourth and fifth edges. First and second MOS transistors are formed in the active area and have first and second gate electrodes. The first and second gate electrodes are parallel to one another and has a source/drain region disposed therebetween. The current/leakage prevention portion is defined by the lengths of first and second gate electrodes. A portion of the length of the second gate electrode which extends beyond a virtual line of the fifth edge is equal in length to the length of the first gate electrode from the fourth edge to a first end thereof.

Through the structure of the claimed invention a) having an active area with a recess and first and second gate electrodes having a source/drain region disposed

therebetween and b) having a portion of length of the second gate electrode which extends beyond a virtual line of the fifth edge equal in length to the length of the first gate electrode extending beyond the fourth edge, as claimed in claims 25 and 31, the claimed invention provides a semiconductor device and method thereof which prevents the occurrence of current leakage between source/drain region so that the function of the MOS transistor can be maintained. The prior art does not show, teach or suggest the invention as claimed in claims 25 and 31.

Claims 25-33 were rejected under 35 U.S.C. §103 as being unpatentable over *Shou et al.* (U.S. Patent No. 5,811,859) in view of *Bergemont* (WO 94/29898) and *Jassowski et al.* (U.S. Patent No. 5,668,389).

Shou et al. appears to disclose in FIG. 3, a LSI pattern of inverted amplifier INV consisting of 3 stages MOS invertors, I1, I2 and I3. For the invertors I1 and I2, there are shaped a common P-type semiconductor layer PL1 and a common N-type semiconductor layer NL1. P-type semiconductor layer PL2 and N-type semiconductor layer NL2 are shaped for I3. Drain voltage Vdd and source voltage Vss are connected to PL1 and NL1 through contacts C1 and C2. A contact is a metal part passing through in semiconductor layer in the direction of thickness, for electrical connection. The drain voltage Vdd and source voltage Vss are connected to PL2 and NL2 through contacts C7 and C8. The semiconductor layers PL1 and NL1 are provided with contacts C3 and C4 for an output from the first stage, respectively, and are provided with contacts C5 and C6 for an output from the second stage, respectively. The semiconductor layers PL2 and NL2 are provided with contacts C9 and C10 for an output from the third stage, respectively, from which an output is introduced through a poly-silicon portion PS toward the next stage. A strangulation portion S1 is provided between the contacts C1 and C5 in the

semiconductor layer PL1, and a strangulation portion S3 is provided between the contacts C2 and C6 in the semiconductor layer NL1. A strangulation portion S2 is provided between contacts C7 and C9 in the semiconductor layers PL2, and a strangulation portion S4 is provided between contacts C8 and C10 in the semiconductor layer NL2. These strangulation means S1 and S3 limit an electric current of the output of inverter I2, and it simultaneously decreases parasitic capacity of a transistor included in the inverter I2 by decreasing electric currency. (col. 2, line 44 through col. 3, line 8)

Thus, *Shou et al.* merely discloses strangulation portions S1, S2 each provided with a gate G. Thus, nothing in *Shou et al.* shows, teaches or suggests first and second gate electrodes having a portion of the length of the second gate electrode which extends beyond a virtual line of the fifth edge equal in length to the length of the first gate electrode extending beyond the fourth edge, as claimed in claims 25 and 31. Nor does *Shou et al.* show, teach or suggest the second length as claimed in claims 28 and 34. Rather, *Shou et al.* strangulations S1 and S2.

Bergemont appears to disclose, according to conventional single poly integrated circuit fabrication techniques, all of the polysilicon lines in the circuit are defined simultaneously utilizing a single mask step. That is, a layer of polysilicon (poly1) is first formed over the entire device structure. A poly 1 photoresist mask is then formed and pattern to define the underlying polysilicon. A single etch step is then performed to define individual poly1 lines. As shown in Fig. 1A, the fabrication process specification defines the desired offset distances "a" and "b" for the "end caps" of the individual polysilicon lines in both the x-direction and the y-direction, respectively. However, rather than the substantially rectangular (90^0) geometry shown in Fig. 1A, in reality, the final geometry of both the field oxide island 10 and

the end cap of the polysilicon line 12 is more "rounded", as shown in Fig. 1B. The field oxide rounding effect is inherent to the type of field isolation and photolithographic process used. The poly end cap rounding effect is inherent to the photolithography of small polysilicon lines. As shown in Fig. 1B, these physical rounding effects result in a reduced width of the polysilicon lines 10 at the poly1/field oxide interface. Thus, when the poly1 line is used as a self-aligned mask for the implementation of dopant to create the source and drain regions of MOS transistors in the circuit, the channel length of the MOS device is reduced, leading to undesirable current leakage from one side of the poly1 to the other. Any misalignment of the poly1 mask further exacerbates this leakage problem, as shown in Fig. 1C. To avoid this problem, prior art techniques rely on larger design rules. That is, design rules for the length of the poly end cap, the distance between the poly end cap and the parallel edge of the field oxide, and the width of the poly1 line all may be increased. These steps insure that the channel length of each of the MOS devices in the circuit is greater than an acceptable minimum required to prevent leakage.

Thus, *Bergemont* merely discloses end caps. Nothing in *Bergemont* shows, teaches or suggests the configuration of the active area and leakage prevention portion as claimed in claims 25, 28, 31 and 34. Nor does *Bergemont* show, teach or suggest first and second electrodes having a portion of length of the second gate electrode which extends beyond a virtual line of the fifth edge equal in length to the length of the first gate electrode extending beyond the fourth edge, as claimed in claims 25 and 31. Also *Bergemont* does not show, teach or suggest the second length as claimed in claims 28 and 34. Rather, *Bergemont* merely discloses providing end caps.

Jassowski et al. merely discloses individual cells 9 in each row align to utilize power buses 12 and 14. As shown in Figure 2 of *Jassowski et al.* attached to the June 29, 2005 amendment, gate G' intervenes between gate G4 and gate G3. Thus nothing in *Jassowski* shows, teaches or suggests first and second gate electrodes having a portion of length of the second gate electrode which extends beyond a virtual line of the fifth edge equal in length to the length of the first gate electrode extending beyond the fourth edge, as claimed in claims 25 and 31 nor the second length as claimed in claims 28 and 34.

The combination of *Shou et al.*, *Bergemont* and *Jassowski et al.* would merely suggest that each gate G of *Shou et al.* provided in the strangulation regions S1 and S2 are provided with end caps as taught by *Bergemont* while having edges as taught by *Jassowski et al.* Nothing in the combination of the references shows, teaches or suggests first and second gate electrodes having a portion of length of the second gate electrode which extends beyond a virtual line of the fifth edge equal in length to the length of the first gate electrode extending beyond the fourth edge, as claimed in claims 25 and 31 nor the second length as claimed in claims 28 and 34. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 25, 28, 31 and 34 under 35 U.S.C. §103.

Claims 26-27, 29-30 and 32-33 depend from claims 25 and 31 and recite additional features. Applicants respectfully submit that claims 26-27, 29-30 and 32-33 would not have been obvious within the meaning of 35 U.S.C. §103 over *Shou et al.*, *Bergemont* and *Jassowski et al.* at least for the reasons as set forth above. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 26-27, 29-30 and 32-33 under 35 U.S.C. §103.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BUCHANAN INGERSOLL PC

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